IN THE CLAIMS:

Please amend Claims 1, 14, 22, and 29 - 32 as follows.

1. (Currently Amended) A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a series of layers consisting essentially of a barrier layer on said substrate, a noble metal layer on said barrier layer, a protective layer on said noble metal layer, a mask layer on said protective layer, and a patterned resist layer on said mask layer, wherein said protective layer and said mask layer consist essentially of inorganic materials;

b) pattern etching said mask layer using a plasma generated from an etchant gas to expose a portion of said protective layer;

c) removing said patterned resist layer from said mask layer;

d) pattern etching said protective layer to expose a portion of said noble metal layer;

e) heating said noble metal layer to a temperature ranging from about 150°C to about 500°C;

f) pattern etching said noble metal layer using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, and a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof;

g) removing said mask layer from said protective layer; and

h) pattern etching said barrier layer using a plasma generated from an etchant gas, to expose a portion of said substrate.

2. (Previously Presented) The method of Claim 1 wherein, after completion of step g), there is residual noble metal on a surface of said barrier layer, and wherein said method comprises an additional step g-2) after step g), in which said residual noble metal is removed from said barrier layer prior to said step (h) pattern etching of said barrier layer.

3. (Previously Presented) The method of Claim 1 wherein said method comprises an additional step g-2) after step g), in which residual protective layer material is removed from said noble metal layer.

4. (Previously Presented) The method of Claim 1 wherein, after completion of step g), there is residual noble metal on a surface of said barrier layer, and wherein said method comprises an additional step g-2) after step g), in which said residual noble metal and any remaining protective layer material are removed prior to said step (h) pattern etching of said barrier layer.

5. (Previously Presented) The method of Claim 1 wherein said protective layer is removed from said noble metal layer during pattern etching of said barrier layer.

6. (Original) The method of Claim 1 wherein said mask layer comprises CVD SiO_2.

7. (Previously Presented) The method of Claim 2 wherein said mask layer and said substrate each comprises CVD SiO_2.

8. (Original) The method of Claim 4 wherein said mask layer comprises CVD SiO_2.

9. (Previously Presented) The method of Claim 1 wherein said mask layer comprises a compound selected from the group consisting of TEOS, CVD SiO_2, Si_3N_4, BSG, PSG, BPSG, and mixtures thereof.

10. (Original) The method of Claim 1 wherein said barrier layer comprises a compound selected from the group consisting of TiN, TiSiN, Ti, WN, TaN, TaSiN, Ta, and mixtures thereof.

11. (Original) The method of Claim 1 wherein said protective layer comprises a compound selected from the group consisting of TiN, TiSiN, Ti, WN, TaN, TaSiN, Ta, and mixtures thereof.

12. (Cancelled)

13. (Previously Presented) A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a series of layers consisting essentially of a barrier layer on said substrate, a noble metal layer on said barrier layer, an inorganic mask layer on said noble metal layer, and a patterned resist layer on said mask layer;

b) pattern etching said mask layer using a plasma generated from an etchant gas to expose a portion of said noble metal layer;

c) removing said patterned resist layer from said mask layer;

d) heating said noble metal layer to a temperature ranging from about 150°C to about 500°C;

e) pattern etching said noble metal layer using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, and a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof;

f) removing said mask layer from said etched noble metal layer; and

g) pattern etching said barrier layer using a plasma generated from an etchant gas to expose a portion of said substrate.

14. (Currently Amended) A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a series of layers consisting essentially of a barrier layer on said substrate , a noble metal layer on said barrier layer, a protective layer on said noble metal layer, a mask layer on said protective layer, and a patterned resist layer on said mask layer, wherein said protective layer and said mask layer consist essentially of inorganic materials;

b) pattern etching said mask layer using a plasma generated from an etchant gas to expose a portion of said protective layer;

c) removing said patterned resist layer from said mask layer;

d) pattern etching said protective layer to expose a portion of said noble metal layer ;

e) pattern etching said noble metal layer using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, and a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof, at a substrate temperature between about 150°C and about 500°C;

f) pattern etching said barrier layer using a plasma generated from an etchant gas to expose a portion of said substrate; and

g) removing said mask layer from said protective layer.

15. (Original) The method of Claim 14 wherein said barrier layer comprises a compound selected from the group consisting of TiN, TiSiN, Ti, WN, TaN, TaSiN, Ta, and mixtures thereof.

16. (Original) The method of Claim 14 wherein said protective layer comprises a compound selected from the group consisting of TiN, TiSiN, Ti, WN, TaN, TaSiN, Ta, and mixtures thereof.

17. (Cancelled)

18. (Previously Presented) The method of Claim 14 wherein said mask layer comprises a compound selected from the group consisting of TEOS, CVD SiO_2, Si_3N_4, BSG, PSG, BPSG, and mixtures thereof.

19. (Previously Presented) A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a series of layers consisting essentially of an etch-stop layer on said substrate, a barrier layer on said etch-stop layer, a noble metal layer on said barrier layer, an inorganic mask layer directly overlying said noble metal layer, and a patterned resist layer on said mask layer;

b) pattern etching said mask layer using a plasma generated from an etchant gas to expose a portion of said noble metal layer;

c) removing said patterned resist layer from said mask layer;

d) pattern etching said noble metal layer using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof, and an additive gas selected from the group consisting of HBr, BCl_3, and mixtures thereof, at a substrate temperature between about 150°C and about 500°C;

e) pattern etching said barrier layer to expose a portion of said etch-stop layer; and

f) removing said mask layer from said etched noble metal layer.

20. (Previously Presented) The method of Claim 19 wherein said method additionally comprises the step of etching said etch-stop layer.

21. (Previously Presented) The method of Claim 19 wherein said mask layer comprises a compound selected from the group consisting of TEOS, CVD SiO_2, Si_3N_4, BSG, PSG, BPSG, and mixtures thereof.

22. (Currently Amended) A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a barrier layer, a noble metal layer on said barrier layer, a first mask layer directly overlying said noble metal layer, a second mask layer directly overlying said first mask layer, and a patterned resist layer on said second mask layer, wherein said first mask layer and said second mask layer consist essentially of inorganic materials;

b) pattern etching said second mask layer using a plasma generated from an etchant gas to expose a portion of said first mask layer;

c) pattern etching said first mask layer to expose a portion of said noble metal layer;

d) removing said patterned resist layer from said second mask layer;

e) pattern etching said noble metal layer and <u>etching</u> said second mask layer <u>surface</u> using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, and a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof, at a substrate temperature between about 150°C and about 500°C;

f) pattern etching said barrier layer; and

g) removing <u>any residue of said second mask layer and</u> said first mask layer from said etched noble metal layer.

23. (Previously Presented) The method of Claim 22 wherein said patterned resist layer is removed from said second mask layer during etching of said first mask layer.

24. (Previously Presented) The method of Claim 22 wherein said first mask layer comprises a compound selected from the group consisting of Si_3N_4, BSG, PSG, BPSG, and mixtures thereof.

25. (Original) The method of Claim 22 wherein said second mask layer comprises a compound selected from the group consisting of CVD SiO_2, TEOS, Si_3N_4, BSG, PSG, BPSG, SiC, and mixtures thereof.

26. (Cancelled)

27. (Original) The method of Claim 22 wherein said second mask layer has a thickness ranging from about 500Å to about 4000Å.

28. (Cancelled)

29. (Currently Amended) ~~The method of Claim 1, wherein said etchant gas also contains~~ A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a series of layers consisting essentially of a barrier layer on said substrate, a noble metal layer on said barrier layer, a protective layer on said noble metal layer, a mask layer on said protective layer, and a patterned resist layer on said mask layer, wherein said protective layer and said mask layer consist essentially of inorganic materials;

b) pattern etching said mask layer using a plasma generated from an etchant gas to expose a portion of said protective layer;

c) removing said patterned resist layer from said mask layer;

d) pattern etching said protective layer to expose a portion of said noble metal layer;

e) heating said noble metal layer to a temperature ranging from about 150°C to about 500°C;

f) pattern etching said noble metal layer using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, a gas selected from the group consisting of a

noble gas, nitrogen, and mixtures thereof, and an additive gas selected from the group consisting of HBr, BCl_3, $SiCl_4$ and mixtures thereof ;

g) removing said mask layer from said protective layer; and

h) pattern etching said barrier layer using a plasma generated from an etchant gas, to expose a portion of said substrate.

30. (Currently Amended) ~~The method of Claim 13, wherein said etchant gas also contains~~ A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a series of layers consisting essentially of a barrier layer on said substrate, a noble metal layer on said barrier layer, an inorganic mask layer on said noble metal layer, and a patterned resist layer on said mask layer;

b) pattern etching said mask layer using a plasma generated from an etchant gas to expose a portion of said noble metal layer;

c) removing said patterned resist layer from said mask layer;

d) heating said noble metal layer to a temperature ranging from about 150°C to about 500°C;

e) pattern etching said noble metal layer using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof, and an additive gas selected from the group consisting of HBr, BCl_3, $SiCl_4$ and mixtures thereof ;

f) removing said mask layer from said etched noble metal layer; and

g) pattern etching said barrier layer using a plasma generated from an etchant gas to expose a portion of said substrate.

31. (Currently Amended) ~~The method of Claim 14, wherein said etchant gas also contains~~

A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a series of layers consisting essentially of a barrier layer on said substrate, a noble metal layer on said barrier layer, a protective layer on said noble metal layer, a mask layer on said protective layer, and a patterned resist layer on said mask layer, wherein said protective layer and said mask layer consist essentially of inorganic materials;

b) pattern etching said mask layer using a plasma generated from an etchant gas to expose a portion of said protective layer;

c) removing said patterned resist layer from said mask layer;

d) pattern etching said protective layer to expose a portion of said noble metal layer ;

e) pattern etching said noble metal layer using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof, and an additive gas selected from the group consisting of HBr, BCl_3, $SiCl_4$ and mixtures thereof , at a substrate temperature between about 150°C and about 500°C;

f) pattern etching said barrier layer using a plasma generated from an etchant gas to expose a portion of said substrate; and

g) removing said mask layer from said protective layer.

32. (Currently Amended) ~~The method of Claim 22, wherein said etchant gas also contains~~ A method of pattern etching a noble metal layer to form an electrode in a RAM capacitor, comprising the steps of:

a) providing a substrate supporting a barrier layer, a noble metal layer on said barrier layer, a first mask layer directly overlying said noble metal layer, a second mask layer directly overlying said first mask layer, and a patterned resist layer on said second mask layer, wherein said first mask layer and said second mask layer consist essentially of inorganic materials;

b) pattern etching said second mask layer using a plasma generated from an etchant gas to expose a portion of said first mask layer;

c) pattern etching said first mask layer to expose a portion of said noble metal layer;

d) removing said patterned resist layer from said second mask layer;

e) pattern etching said noble metal layer and etching said second mask layer surface using a plasma generated from an etchant gas consisting essentially of a halogen containing gas, a gas selected from the group consisting of a noble gas, nitrogen, and mixtures thereof, and an additive gas selected from the group consisting of HBr, BCl_3, $SiCl_4$ and mixtures thereof , at a substrate temperature between about 150°C and about 500°C;

f) pattern etching said barrier layer; and

g) removing any residue of said second mask layer and said first mask layer from said etched noble metal layer.